REMARKS

This amendment responds to the office action mailed September 10, 2003. In the office action the Examiner:

- rejected claims 1, 6-9, 17, 22, 23, 28 and 30-32 under 35 U.S.C. 102(b) as anticipated by Dillon et al. (US 5,663,661); and
- objected to claims 2-5, 10-16, 18-21, 24-27 and 29 as being dependent upon a rejected base claim.

After entry of this amendment, the pending claims are: claims 1-32.

To get directly to the main point, Figure 6 of Dillon does not show a slave device. Rather, looking at Figure 1 of Dillon, there is shown a master that is coupled to multiple slaves. Further, in Figure 1 all the slaves are coupled to the master via a single interface on the master. The entire purpose of Figure 6 of Dillon is to show another version of the master that has two ports or interfaces for connecting to slave devices. In other words, Figure 6 represents another embodiment in which the circuitry of Figure 6 replaces the Master 110 in Figure 1. Socket 1 (617) and Socket 2 (615) in Dillon's Figure 6 are the two ports of the dual-channel Master for connecting to two sets of slave devices. The Sockets 615, 617 are literally "sockets" into which memory modules are plugged (see col. 12, lines 10-12). Each memory module (i.e., a module containing slave devices) 120 has the bus lines and slaves shown in Figure 1 as contained with a module 120. Figure 1 has two memory modules coupled to a single socket or port of a Master 110, while Figure 6 provides a Master with two sockets for connecting to two modules of slave devices.

The clk3 and clk4 signals in Dillon's Figure 6 are conveyed via the sockets 615, 617 and become the "clk from master A" and "clk from master B" signals when modules are plugged into sockets 615 and 617. The slave devices, as shown in Figure 1, only receive the "clk from master A/B" and "clk to master A/B" signals, and do not receive the clk3 and clk4 signals in addition. Restated, the slave devices in Dillon receive two clock signals, not three, and furthermore do not receive a clock signal and two distinct phase signals.

The circuitry shown in Dillon's Figure 6, is therefore part of the Master device in a master-slave system.

Claim 1 requires that a slave device receive three distinct signals, a clock signal and two different phase signals on three distinct nodes. The slave devices 125 in Dillon receive only two signals: a clock to master (ctm) and a clock from mater (cfm). Dillon does not use

the clock and two phase signals methodology or architecture of the present invention. Therefore claim 1 and its dependent claims are neither anticipated nor made obvious by Dillon.

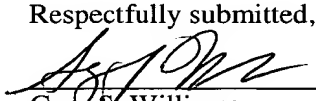
Claim 17 also requires that a slave device receive a clock signal and two different phase signals, and further requires (A) that the clock and phase-to-master signal be used for transmitting data to a master device and (B) that the clock and phase-from-master signal be used for receiving data to a master device. In contrast, in Dillon, data is transmitted to the master using just the clock to master signal (ctm), and does not use a clock and a separate phase signal for this purpose. Similarly, in Dillon, data is received from the master using just the clock from master signal (cfm), and does not use a clock and a separate phase signal for this purpose. Therefore at least three aspects of claim 17 are not found in Dillon. As a result, claim 17 and its dependent claims are neither anticipated nor made obvious by Dillon.

Claim 8 also requires that a slave device process data on a data bus in response to three signals: a clock signal, a phase-to-master phase signal and a phase-from-master signal. Since the slave devices in Dillon operate on data using two clock signals, and do not use the three signals required by claim 8, claim 8 is neither anticipated nor made obvious by Dillon.

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at 650 493-4935, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: February 20, 2004



31,066
Gary S. Williams (Reg. No.)

Morgan, Lewis & Bockius LLP
3300 Hillview Avenue
Palo Alto, California 94304
(650) 493-4935